WHAT IS CLAIMD IS:

1. A semiconductor package board comprising:

a metal base plate having an opening suited for receiving therein a semiconductor chip; and

a multilayer wiring film formed on said metal base plate, said multilayer wiring film having a first surface in contact with said metal base plate and mounting thereon a plurality of first metal pads within a region exposed from said opening of said metal base plate.

2. The semiconductor package board according to claim 1, wherein said multilayer wiring film includes a plurality of wiring layers and a plurality of insulating layers alternately stacked upon one another, via holes formed in said plurality of insulating layers for interconnecting said plurality of wiring layers, and a plurality of second metal pads formed on a second surface of said multilayer wiring film opposite to said first surface, and wherein said second metal pads are electrically connected to said first metal pads through said wiring layers and said via holes.

3. The semiconductor package board according to claim 1, wherein said multilayer wiring film has a metallic film in contact with a periphery of said opening of said metal base plate.

4. The semiconductor package board according to claim 1, wherein said multilayer wiring film mounts thereon a thin-film

capacitor between at least one of said first metal pads and said wiring layers.

5. The semiconductor package board according to claim 1, wherein said metal base plate comprises at least one metal selected from the group consisting of stainless steel, iron, nickel, copper, and aluminum, or an alloy thereof.

6. The semiconductor package board according to claim 1, wherein said first metal pads are covered by a surface layer comprising at least one metal selected from the group consisting of gold, tin, and solder, or an alloy thereof.

7. The semiconductor package board according to claim 2, wherein each of said insulating layers comprises one or more of organic resins selected from the group consisting of an epoxy resin, an epoxy acrylate resin, an urethan acrylate resin, a polyester resin, a phenol resin, a polyimide resin, a benzocyclobutene (BCB), and a polybenzoxazole (PBO).

8. The semiconductor package board according to claim 2, further comprising a carrier base mounted on said second surface of said multilayer wiring film and connected to said second metal pads.

9 The semiconductor package board according to claim 8,

wherein said carrier base is connected to said second metal pads either through conductive paste or through an anisotropic conductive film.

10. The semiconductor package board according to claim 8, wherein said carrier base is one of printed circuit board, ceramic board, and organic/inorganic composite board, having at least one wiring layer.

11. The semiconductor package board according to claim 8, wherein said carrier base includes a resistor.

12. The semiconductor package board according to claim 8, wherein said carrier base includes a capacitor.

13. The semiconductor package board according to claim 8, wherein said carrier base is electrically connected to ground.

14. The semiconductor package board according to claim 8, wherein said carrier base mounts thereon a plurality of either solder balls or connector pins on a surface thereof opposite to a surface in contact with said multilayer wiring film, said solder balls or connector pins being electrically connected to said second metal pads through said carrier base.

15. A semiconductor device comprising the semiconductor package

board according to claim 1, and a semiconductor chip disposed within said opening and connected to said first metal pads.

16. The semiconductor device according to claim 15, wherein said semiconductor chip is flip-chip bonded to said first metal pads by a material made of either a metal having a low melting point or a conductive resin.

17. The semiconductor device according to claim 15, wherein said semiconductor chip is connected to said multilayer wiring film by at least one material selected from the group consisting of a metal having a low melting point, an organic resin, and a resin containing a metal.

18. A method for manufacturing a semiconductor package board, comprising the steps of:

forming a plurality of first metal pads on a first surface of a metal base plate;

forming a multilayer wiring film including a plurality of insulating layers and a plurality of wiring layers on said first surface of said metal base plate, said multilayer wiring film having a plurality of second metal pads on a top surface thereof, each of said plurality of second metal pads being electrically connected to respective said first metal pads through said wiring layers; and

forming an opening in said metal base plate suited for receiving therein a semiconductor chip, said opening exposing said first metal

pads.

19. The method as defined in claim 1, further comprising the step of forming a metallic film on said first surface of said metal base plate in a region other than regions where said first metal pads are disposed, said metallic film extending along a periphery of said opening after said opening forming step

20. The method as defined in claim 19, wherein said first metal pads forming step and said metallic film forming step are concurrently conducted.

21. The method according to claim 18, further comprising the step of forming a recess on a second surface of said metal base plate in a region where said opening is to be formed, prior to said first metal pads forming step.

22. The method according to claim 18, further comprising the steps of forming a plurality of another first metal pads on a second surface of said metal base plate, forming another multilayer wiring film on said second surface, and separating said metal base plate into to a first piece having said first surface and a second piece having said second surface.

23. The method according to claim 22, further comprising the step

of bonding a pair of metal plates together to form said metal base plate.

24 The method according to claim 18, wherein said first metal pads forming step includes the steps of forming a first resist mask having a plurality of openings, plating said metal base plate by using said first resist mask as a plating mask to form said first metal pads in said openings, and removing said first resist.

25. The method according to claim 24, wherein said first metal pads forming step includes the step of etching said metal base plate by using said first resist to form a plurality of recesses for receiving therein said first metal pads prior to said plating step.

26. The method according to claim 19, wherein said metallic film forming step includes the step of plating said metal base plate by using a resist mask.

27. The method according to claim 24, wherein said first metal pads forming step includes the step of forming a plurality of solder balls in said openings prior to said plating step.

28. The method according to claim 18, further comprising the step of forming a thin-film capacitor on one of said first metal pads prior to said multilayer wiring film forming step.

29. The method according to claim 18, wherein said multilayer wiring film forming step includes the steps of forming a insulating layer, forming a plurality of via holes in said insulating layer corresponding to said first metal pads, forming alternately a plurality of wiring layers and a plurality of insulating layers, each of said wiring layers including a plurality of interconnections disposed corresponding to said via holes and insulator resin filled between said interconnections, and forming said second metal pads on an outermost surface of said multilayer wiring film.

30. The method according to claim 18, wherein said opening forming step includes the steps of forming a resist exposing a portion of a second surface of said metal base plate, etching said portion of metal base plate by using said resist as a mask to form said opening, and removing said resist.

31. The method according to claim 18, further comprising the step of forming a plurality of solder balls or connection pins on respective said second metal pads.

32. The method according to claim 18, wherein said metal base plate comprises at least one metal selected from the group consisting of stainless steel, iron, nickel, copper, and aluminum, or an alloy thereof.

33. The method according to claim 18, further comprising the step of bonding a carrier base onto a surface of said multilayer wiring film on a side opposite to a surface in contact with said metal base plate.

34. The method according to claim 33, wherein said carrier base is one of a printed circuit board, ceramic board, and organic/inorganic composite board, having at least one wiring layer.

35. The method according to claim 33, wherein said carrier base is bonded to said multilayer wiring film by using any one of an adhesive, thermo-compression, and a chemical reaction.

36. The method according to claim 33, wherein said carrier base is electrically connected to said second metal pads either using conductive paste or an anisotropic conductive film.

37. The method according to claim 33, further comprising the step of forming a plurality of either solder balls or connector pins on a surface of said carrier base so as to be electrically connected to said second metal pads through said carrier base.

38. The method according to claim 33, wherein said carrier base bonding step is carried out prior to said opening forming step.

39. The method according to claim 33, wherein said carrier base

bonding step is carried out after said opening forming step.

40 The method according to claim 33, further comprising the step of connecting a semiconductor chip to said first metal pads.

41. The method according to claim 40, wherein said semiconductor chip is flip-chip bonded to said first metal pads by a material made of either a metal having a low melting point or a conductive resin.

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